AMENDMENTS TO CLAIMS

- Please delete claims 3, 13, and 19.
- Please amend pending claims 1, 11, and 16, as indicated below. A complete listing of all claims and their status in the application are as follows:

1. (currently amended) A method of manufacturing an integrated circuit comprising:

providing a semiconductor substrate having a semiconductor device provided thereon;

forming an ultra-low dielectric constant dielectric layer over the semiconductor substrate, forming the ultra-low dielectric constant dielectric layer deposits a porous material;

forming an opening in the ultra-low dielectric constant dielectric layer;

forming a dielectric liner to line the opening in the ultra-low dielectric constant dielectric layer, forming the dielectric liner deposits a nonporous material;

depositing a barrier layer to line the dielectric liner; and

depositing a conductor core over the barrier layer to fill the barrier layer and connect to the semiconductor device.

2. (original) The method of manufacturing an integrated circuit as claimed in claim 1 wherein forming the dielectric liner forms a material with a dielectric constant higher than the dielectric constant of the ultra-low dielectric constant dielectric layer.

3. (canceled)

4. (original) The method of manufacturing an integrated circuit as claimed in claim 1 wherein forming the dielectric liner deposits a non-porous conformal liner.

5. (original) The method of manufacturing an integrated circuit as claimed in claim 1 wherein depositing the barrier layer uses a material selected from a group consisting of tantalum, titanium, tungsten, a compound thereof, and a combination thereof.

6. (original) A method of manufacturing an integrated circuit comprising:

providing a semiconductor substrate having a semiconductor device provided thereon;

depositing an ultra-low dielectric constant dielectric layer over the semiconductor substrate, depositing the ultra-low dielectric constant dielectric layer deposits a dielectric material having pores and a dielectric constant under 2.5;

forming an opening in the ultra-low dielectric constant dielectric layer;

depositing a dielectric liner to line the opening in the ultra-low dielectric constant dielectric layer, depositing the dielectric liner deposits a non-porous dielectric material;

depositing a barrier layer to line the dielectric liner; and

depositing a conductor core over the barrier layer to fill the barrier layer and connect to the semiconductor device.

7. (original) The method of manufacturing an integrated circuit as claimed in claim 6 wherein depositing the dielectric liner deposits a material with a dielectric constant under 4.2.

8. (original) The method of manufacturing an integrated circuit as claimed in claim 6 wherein depositing the dielectric liner deposits a material with a dielectric constant under 3.9.

9. (original) The method of manufacturing an integrated circuit as claimed in claim 6 wherein:

depositing the ultra-low dielectric constant dielectric layer deposits a material having pores; and

depositing the dielectric liner deposits a material filling the pores in the opening and forming a liner which is conformal to the opening.

10. (original) The method of manufacturing an integrated circuit as claimed in claim 6 wherein depositing the barrier layer uses a material selected from a group consisting of tantalum, titanium, tungsten, a compound thereof, and a combination thereof.

11. (currently amended) An integrated circuit comprising:

a semiconductor substrate having a semiconductor device provided thereon;

an ultra-low dielectric constant dielectric layer over the semiconductor substrate, the ultra-low dielectric constant dielectric layer having an opening provided therein, the ultra-low dielectric constant dielectric layer is a porous material;

dielectric liner lines the opening in the ultra-low dielectric constant dielectric layer, the dielectric liner is a nonporous material;

a barrier layer lines the dielectric liner; and

a conductor core over the barrier layer fills the barrier layer and connects to the semiconductor device.

12. (original) The integrated circuit as claimed in claim 11 wherein the dielectric liner is a material with a dielectric constant higher than the dielectric constant of the ultra-low dielectric constant dielectric layer.

13. (canceled)

14. (original) The integrated circuit as claimed in claim 11 wherein the dielectric liner is a non-porous conformal liner.

15. (original) The integrated circuit as claimed in claim 11 wherein the barrier layer is a material selected from a group consisting of tantalum, titanium, tungsten, a compound thereof, and a combination thereof.

16. (currently amended) An integrated circuit comprising:

a semiconductor substrate having a semiconductor device provided thereon;

an ultra-low dielectric constant dielectric layer over the semiconductor substrate, the ultra-low dielectric constant dielectric layer is a dielectric material having a dielectric constant under 2.5 and having an opening in the ultra-low dielectric constant dielectric layer, the ultra-low dielectric constant dielectric layer is a porous material;

a dielectric liner lines the opening in the ultra-low dielectric constant dielectric layer, the dielectric liner is a dielectric material having a dielectric constant higher than 2.2, the dielectric liner is a material which fills the pores in the opening and forms a liner which is conformal to the opening;

a barrier layer lines the dielectric liner; and

a conductor core over the barrier layer fills the barrier layer and connects to the semiconductor device.

17. (original) The integrated circuit as claimed in claim 16 wherein the dielectric liner is a material with a dielectric constant under 4.2.

18. (original) The integrated circuit as claimed in claim 16 wherein the dielectric liner is a material with a dielectric constant under 3.9.

19. (canceled)

20. (original) The integrated circuit as claimed in claim 16 wherein the barrier layer is a material selected from a group consisting of tantalum, titanium, tungsten, a compound thereof, and a combination thereof.